## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

1

Dmitriy Rumynin et al.

Title:

PARALLEL COUNTER AND A LOGIC CIRCUIT FOR PERFORMING MULTIPLICATION

Docket No.:

1365.051US1 ,

Filed: Examiner: July 27, 2001 Unknown

Serial No.: 09/917,257

Due Date: N/A

Group Art Unit: 2121

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Commissioner for Patents Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

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- A return postcard.
- $\frac{X}{X}$   $\frac{X}{X}$   $\frac{X}{X}$ An Information Disclosure Statement (1 pg.), Form 1449 (2 pgs.), and copies of 36 cited documents.
- International Search Report for PCT/GB02/01343, mailed December 27, 2002 (4 pgs.).
- International Search Report for PCT/GB01/04455, mailed October 7, 2002 (9 pgs.).
- International Search Report for PCT/GB01/03415, mailed November 15, 2002 (10 pgs.).

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 12 day of March, 2003.

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(GENERAL)

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

S/N 09/917257

Dmitriy Rumynin et al.

Examiner:

Unknown

2121

Serial No.:

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**MULTIPLICATION** 

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## INFORMATION DISCLOSURE STATEMENT

MAR 2 0 2003

Assistant Commissioner for Patents Washington, D.C. 20231

**Technology Center 2100** 

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 et. seq., the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Account No. 19-0743 in order to have this Information Disclosure Statement considered.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

DMITRIY RUMYNIN ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. Box 2938
Minneapolis, MN 55402
612-349-9587

Date // March 200

Timothy B Clise

Reg. No. 40,95

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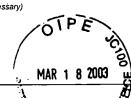
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## Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)



Complete if Known		
Application Number	09/917,257	
Filing Date	July 27, 2001	
First Named Inventor	Rumynin, Dmitriy	RECEIVED
Group Art Unit	2121	MAD 9 A 2002
Examiner Name	Unknown	MAR 2 0 2003

Attorney Docket No: 1365.051US1 Sheet 1 of 2

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	OTH	ER DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Cite Include nam Initials* No 1 (book, m		Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
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**EXAMINER** 

**DATE CONSIDERED** 

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ir the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number. Substitute for form 1449A/PTO Complete if Known INFORMATION DISCLOSURE 09/917,257 **Application Number** STATEMENT BY APPLICANT July 27, 2001 Filing Date (Use as many sheets as necessary) RECEIVED Rumynin, Dmitriy **First Named Inventor** 2121 **Group Art Unit** MAR 1 8 2003 MAR 2 0 2003 Unknown **Examiner Name** Technology Center 2100 Attorney Docket No: 1365.051US1

TRADE Sheet 2 of 2

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item Examiner (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), Initials\* publisher, city and/or country where published. (1965), pp. 118-125 DEBNATH, D., "Minimization of AND-OR-EXOR Three-Level Networks with AND Gate Sharing", IEICE Trans. Inf. & Syst., Vol. E80-D, No. 10, (1997), pp. 1001-1008 DRECHSLER, R., et al., "Sympathy: Fast Exact Minimization of Fixed Polarity Reed-Muller Expressions for Symmetric Functions", IEEE, (1995), pp. 91-97 DRECHSLER, R., et al., "Sympathy: Fast Exact Minimization of Fixed Polarity Reed-Muller Expressions for Symmetric Functions", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, No. 1, (1997), pp. 1-5 FLEISHER, H., "Combinatorial Techniques for Performing Arithmetic and Logical Operations", IBM Research Center, RC-289, Research Report, (July 18, 1960), pp. 1-20 FOSTER, CAXTON, et al., "Counting Responders in an Associative Memory", The Institute of Electrical and Electronics Engineers, Inc., Reprinted, with permission, from IEEE Trans. Comput. C-20:1580-1583, (1971), pp. 86-89 HO, I., et al., "Multiple Addition by Residue Threshold Functions and Their Representation By Array Logic", The Institute of Electrical and Electronics Engineers, Inc., Reprinted, with permission from IEEE Trans. Comput. C-22: 762-767, (1973), pp. 80-85 JONES, ROBERT, et al., "Parallel Counter Implementation", IEEE, (1992), pp. 381-385 NIENHAUS, H., "Efficient Multiplexer Realizations of Symmetric Functions", IEEE, (1981), pp. 522-525 OKLOBDZIJA, V.G., et al., "Improving Multiplier Design by Using Improved Column Compression Tree and Optimized Final Adder in CMOS Technology", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 3, No. 2, (1995), pp. 292-301 SWARTZLANDER, JR., EARLE, "Parallel Counters", Institute of Electrical and Electronic Engineers, Inc., Reprinted, with permission from IEEE Trans. Comput. C-22:1021-1024, (1973), pp. 90-93 VASSILIADIS, S., et al., "7/2 Counters and Multiplication with Threshold Logic", IEEE, (1997), pp. 192-196 WALLACE, C., "A Suggestion for a Fast Multiplier", IEEE Transactions on Electronic Computers, (1964), pp. 14-17 ZURAS, D, et al., "Balanced Delay Trees and Combinatorial Division in VLSI", IEEE Journal of Solid State Circuits, SC-21, IEEE Inc, New York, Vol. SC-21, No. 5, (1986), pp. 814-819

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